AS/6100 NOTES: THE DIFFERENCE IS THE TECHNOLOGY

The AS/6100 is implemented using state-of-the-art emitter-coupled logic Custom Logic Array (ECLA) technology. The ECLA is a Very Large Scale Integration (VLSI) device that bridges the gap between custom-designed VLSI and standard off-the-shelf devices.

The ECLA starts as a substrate of unconnected transistors and resistors. The logic designer can specify which groups of these transistors are connected to form logic cells containing elements such as AND gates, Flip-Flops, and Multiplexers. The designer then specifies how these cells are connected to perform the required logic function. The substrate is common among all ECLAs and can therefore be made in large quantities at a favorable price.

The ECLA provides the AS/6100 with excellent reliability and serviceability. The use of ECLAs means less heat to dissipate, fewer parts, and fewer connections. This increases not only reliability but also performance; since the AS/6100 is small, it has shorter interconnections and, thus, reduced signal-delay times. The improved serviceability comes from the fewer Field-Replaceable Units (FRUs) which are a result of the high logic density of ECLAs. Built-in diagnostic aids will quickly isolate the failing Field Replaceable Unit (FRU).

STEP 1: Logic Design

The project engineers responsible for each functional unit in the AS/6100 select appropriate hardware for the ECLA. These selections are reviewed by all the project engineers and managers. Two engineers are then assigned to develop the detail design of each ECLA. One has primary responsibility; the other serves to double-check the first (while holding primary responsibility for a different ECLA). After the detail design is completed, it is again reviewed. Once approved, the Computer-Aided Design system performs further checks, after which the ECLA development path splits. The design drafting department takes the detail design and produces placement and interconnection information on our independent graphics system. At the same time, the design engineer creates a set of test patterns using a software simulation of his design. There follows a final review and double-check, after which the graphics information (called a MASK tape) and the test patterns are sent out for fabrication.

In designing the AS/6100, ECLAs were used primarily for two purposes: machine speed enhancements and logic reduction. For example, one of the most speed-critical circuits in the AS/6100 is the High-Speed Buffer Index Array Compare. The operational speed of this circuit was almost doubled through use of the ECLA; each ECLA replaces about 19 standard ECL ICs.

At the other end of the spectrum, the Mover logic in the CPU benefited from ECLA in that two ECLA devices replaced about 172 standard ECL ICs. Through the use of these Custom Logic Arrays, we have achieved a replacement average of one ECLA for every 50 ECL ICs.

Designing the ECLA was a comprehensive and painstaking process. Since it is extremely difficult to change the design of an ECLA once it is "cast in silicon," a great deal of time and effort is spent in the simulated design phase to ensure functional correctness before the design becomes a chip.

STEP 2: Fabrication

A four-inch silicon wafer with pre-etched substrate is selected and the placement and interconnection information (from the MASK tape) used to place the final layers of metal interconnection on it. Following this processing, the dozens of ECLAs on each wafer are tested, sectioned, mounted on a ceramic carrier, and retested. The testing uses both predefined voltage and current parameters as well as the logic test patterns generated by the design engineer.

STEP 3: System Test

Once the parts return to San Diego, we check the ECLAs using a computerized IC tester, and then perform extensive system-level tests. After verifying that they meet all of our requirements, the design engineer builds a test circuit which permits his design to be tested in a system simulator.

Summary: Measure of Success

Our success rate in ECLA design is remarkably high. Due to the care taken early in the design process, so far less than 2% of the ECLAs require redesign. Our procedures have enabled us to find problems and correct them with no impact on the overall design process.

As a testament to our efforts, our ECLA vendors think so highly of one of our designs that they have selected it to be a standard product offering. The Arithmetic Logic Unit (ALU) ECLA design will thus be not only in the AS/6100 but may also end up in industry-wide use.

In summary, the ECLA design team is on the leading edge of VLSI Custom Logic Array technology being used in a commercially-available processor. The AS/6100 is a significant steppingstone in the use of even denser VLSI in products in the future.

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